EPSRC Centre for Innovative Manufacturing in

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Self-repairing Electronic Systems

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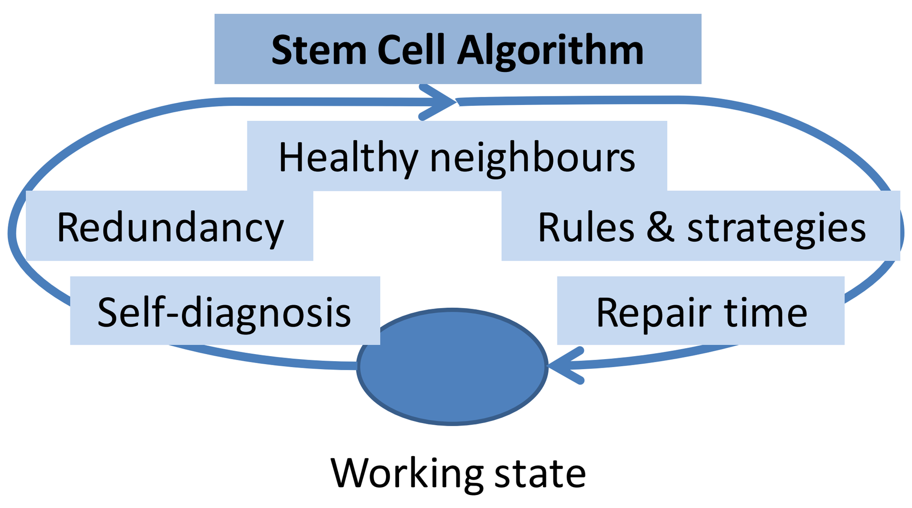
Introduction

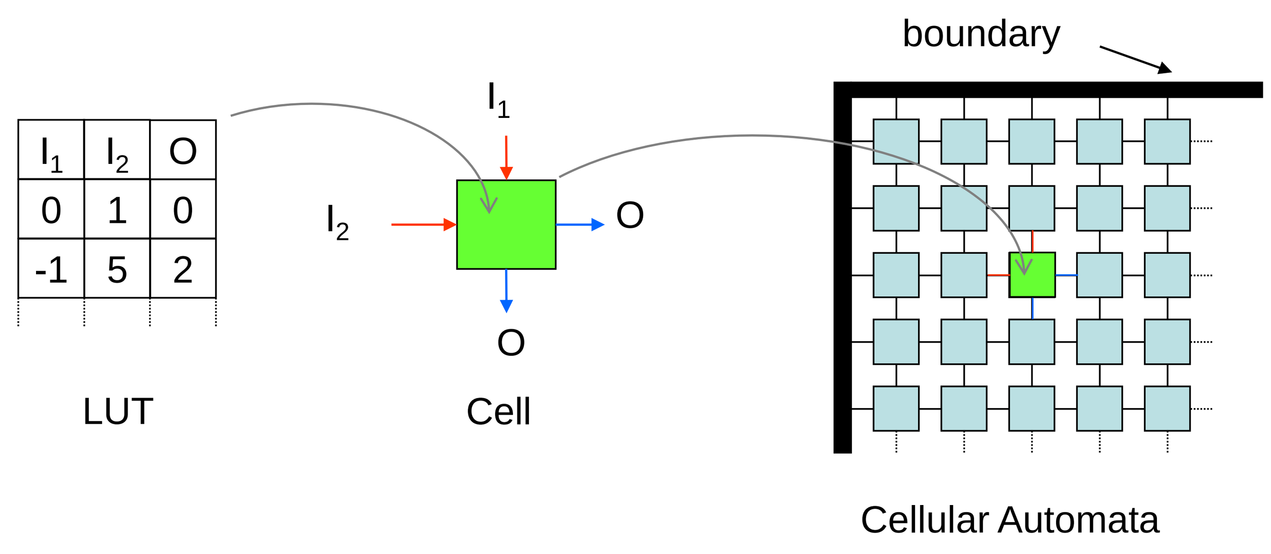
Drawing inspiration from the ***self-healing*** ability of biological cellular systems, we suggest that a stem cell algorithm can be used to ***self-organise*** an array of identical ***computing cells*** that, in the event of local failure, is capable of ***self-repair***. This is achieved by enlisting ***redundant cells*** to replace the faulty ones.



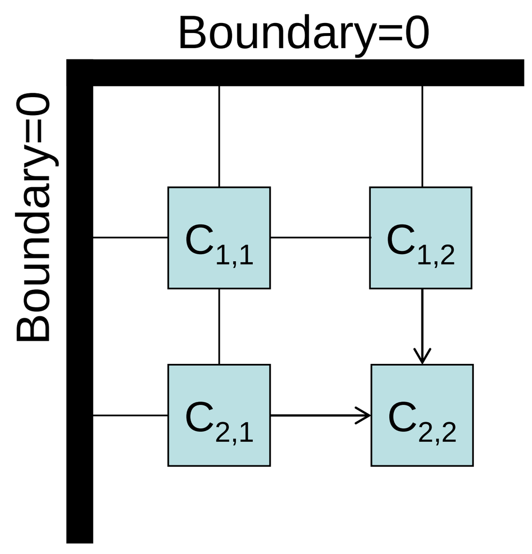
The Cellular Automata (CA)

The cellular automata comprises an array of identical computing cells with external connections, a ***current state*** and a ***LUT*** storing ***rules*** that determine the next state.

An array of these cells represents a computing device whose global state is driven by the ***rules*** and ***boundary values***.



Rules for Convergence



A ***transition function*** determines the ***next state***:

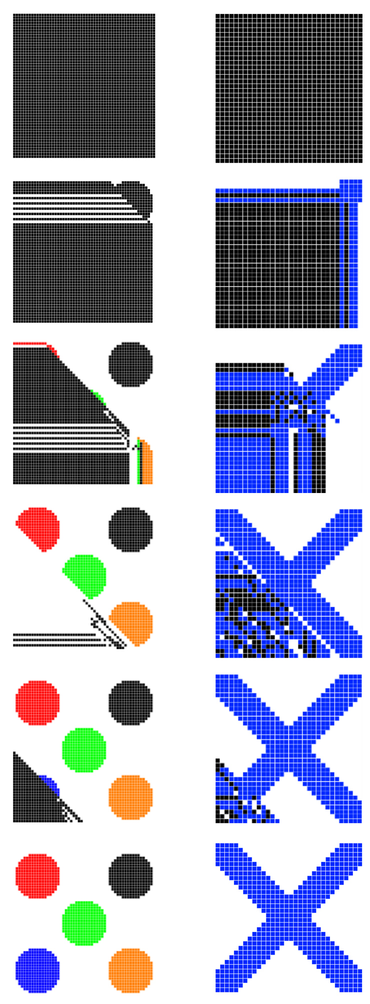
$$C_{i,j,t+1}=nC_{i-1,j,t}+wC_{i,j-1,t}+d$$

Convergence is achieved by ensuring that the next state is independent of the ***initial state***:

$$(\mathbf{I}-\mathbf{A})\mathbf{C}-\mathbf{D}=0$$

$$\begin{bmatrix}1&0&0&0\\-w&1&0&0\\-n&0&1&0\\0&-n&-w&1\end{bmatrix}\begin{bmatrix}C_{1,1}\\C_{1,2}\\C_{2,1}\\C_{2,2}\end{bmatrix}-\begin{bmatrix}d\\d\\d\\d\end{bmatrix}=\begin{bmatrix}0\\0\\0\\0\end{bmatrix}\qquad \mathbf{C}=\begin{bmatrix}C_{1,1}\\C_{1,2}\\C_{2,1}\\C_{2,2}\end{bmatrix}$$

Rules are derived from simultaneous equations

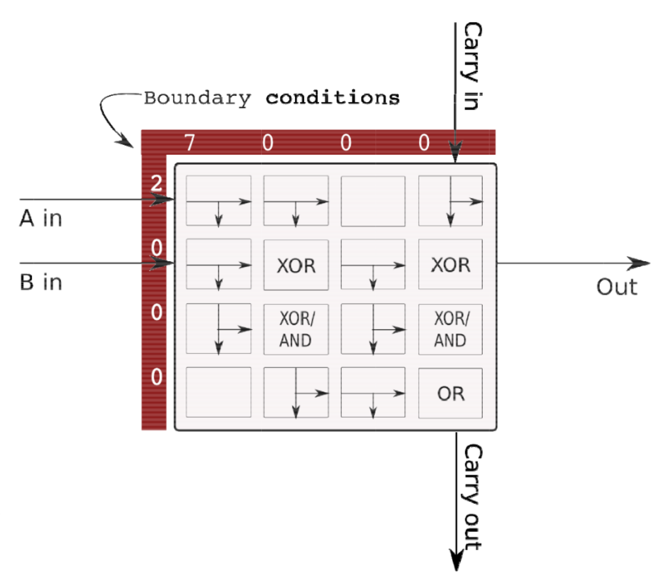


Convergent patterns

Robust logic unit based on cellular automata

A full adder logic unit has been made ***robust*** by implementing high-level functional logic on top of an underlying ***convergent cellular automata*** (CCA)[1].

The CCA ***rules*** guarantee ***self-organisation*** of the underlying adder circuitry, irrespective of the initial arrangement.



CCA full-adder

Future platforms for self-repair

Singe Event Upsets (SEU) cause transient and permanent failures at the cell level of an electronic device. Our cellular automata approach to electronics permits restoration of operation by a) replacing faulty cells using **redundant cells** and b) automatic re-organisation after transient events.

The LEON-SPARC microprocessor[2] is capable of withstanding a SEU at the register level. However this is achieved by triple Modular Redundancy (TMR) on sequential logic blocks and hence only a single fault can be permitted. Our approach is inherently more robust and depends on the number of redundant cells included in the design.

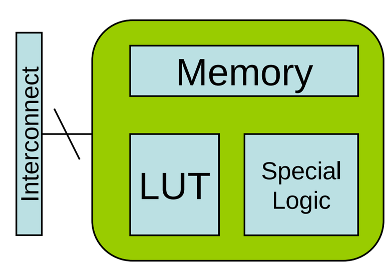
Since current FPGA technology does not provide dynamic re-routing capability during execution, an extension of this work is to define the basis of new a hardware architecture for CCA implementations.

FPGA test platform

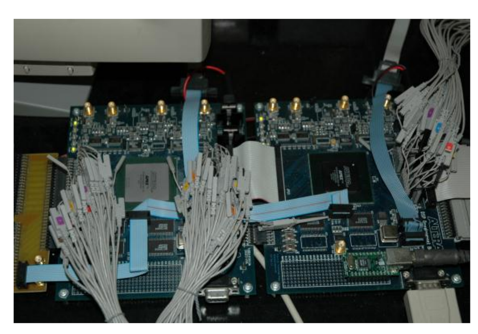
Field-programmable gate arrays (FPGA) comprise a 2-D array of ***logic elements*** (LE), interconnect fabric and global logic.

A LE may be conceptually regarded as being similar to a CCA cell that with the necessary I/O and LUT logic to execute rules.

An Altera Stratix II FPGA was therefore chosen to implement a logic unit based on a CCA.



Logic Element



FPGA Platform

1. D. Jones, R. McWilliam and A. Purvis, New Advanced Technologies, InTech, March 2010.
2. J. Andersson, J. Gaisler and R. Weigand, Data Systems In Aerospace 2010 (DASIA2010), 2010.

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